An Optical Turing Machine for Native Network Processing of Modulated Data

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USC/ISI

IEEE CCW 2012

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OTM Overview

- High-speed communication is multibit optical
  - Want to ***compute*** in that format natively
- USC/ISI's OTM initiative
  - Revisits the assumptions of computation
  - Leverages native optical capabilities
  - Explore unification of comms and computation

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Current Optical Computing

- Analog signal processing
  - Spatial Fourier transforms (lens/lens-like), holography,
    RF-like wave manipulation
  - Limited reconfigurability – static functions
  - Limited composition
- Emerging digital approaches
  - Optical transistors (Miller, *Nature Photonics* ’10), quantum dots
  - Low bandwidth – still one bit per device

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Optical Turing Machine

USC/ISI New Research Initiative

- A new approach to computing
  - – Optical computing…
  - – of high-density (multibit) symbols that natively support high-speed, long-distance transmission
- A fundamental unification
  - – Integrate computation and communication
  - – from the communications viewpoint

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Symbol Encoding

- Single bit per symbol
  - On/off keying (OOK), *e.g.*, of power levels
  - Binary phase-shift keying (BPSK)
  - Binary polarizations
- Multibit encoding
  - Multilevel (multiple power levels)
  - Multiple phases (*N*-PSK, *e.g.,* 4PSK, 16PSK)
- Multidimensional
  - Using more than one physical attribute
  - Implies multibit
  - *E.g.,* QAM (phase and power), OCDMA (phase, wavelength, polarization)

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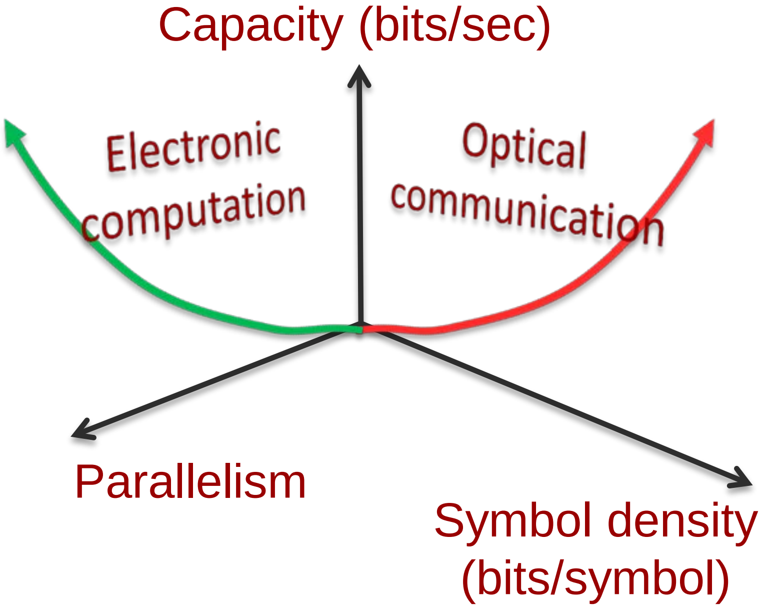
Supporting high speed

- Computation
  - favors electronics for processing
  - electronics uses high parallelism for speed
- Communication
  - ***requires*** optics for distance
  - optics uses high bit density for speed



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Optics Assumptions

- Point-to-point fiber with packet switches
  - Shared channels are limited in range (LAN)
  - Distributed multiaccess requires phase-aligned sources
  - Packet switching ***is*** coordinated multiaccess
- Serial channels
  - Parallel too hard to synchronize

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Computation *vs.* Communication

- High-speed transmission
  - – Currently serial multibit optical encoding
  - – Parallel channels are too costly to synchronize
- High-speed computation
  - – Currently parallel electronic binary encoding
  - – Serial exceeds electronics
- Implication
  - – Compute and transmit in different formats
  - – Conversion is required (“OEO”) and costly

Other Benefits of Optics

Beyond transmission distance

- 60x faster per link
  - Optics: ~100 Gbaud * 4 bits/symbol (16 QAM)
    = 400 Gbps per link
  - Electronics: ~3.25 GHz * 2 bits/cycle (both edges)
    = 6.5 Gbps per link
- Supports similar integration
  - Concurrent streams using a single device
    (2 polarizations x 30 wavelengths)
  - 1/100 devices/chip but 60x streams per device
- Supports serial algorithms
  - Some functions can be simpler
  - 32-bit adder uses ~6 serial elements *vs.* >6,000 parallel

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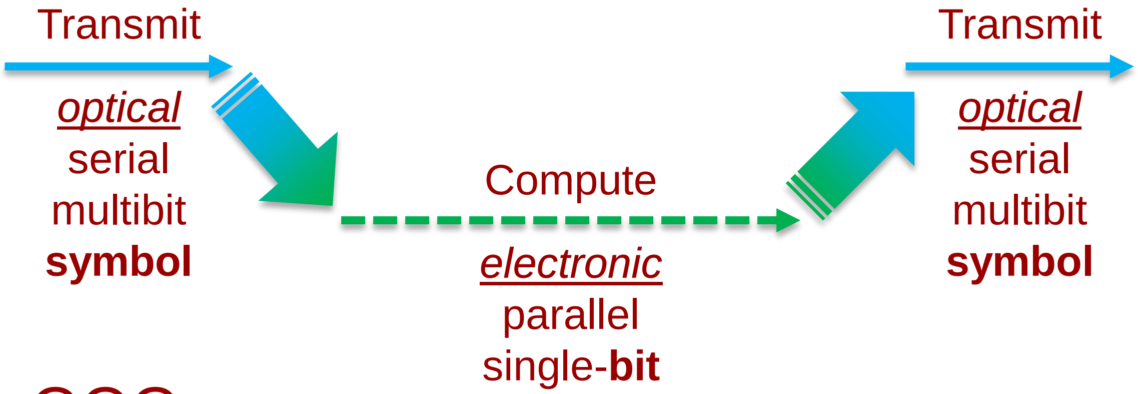
OEO *vs.* SBS

- Optical-electronic-optical (OEO)
  - Really *symbol-bit-symbol* (SBS) from multibit to on-off (OOK)
  - Conversion is expensive in power, complexity, performance



Transmit

optical serial multibit **symbol**

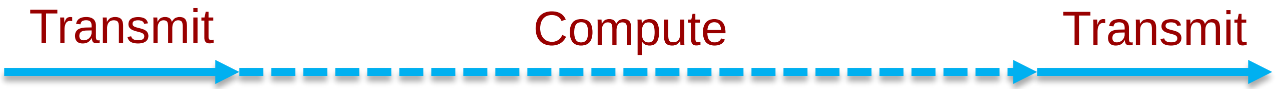
Compute

electronic parallel single-**bit**

Transmit

optical serial multibit **symbol**

- Native OOO
  - Avoid conversion; compute in transmission format



Transmit

Compute

Transmit

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Back to Basics

- Computation
  - – Use state to manage symbol (sequence) translation
- Communication
  - – Exchanging symbols to manage (endpoint) state
- These are related
  - – Both use state
  - – Both “translate” symbols
- Hypothesis:
  - – What if both could share one encoding?

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Native Multibit-symbol Support

- Explore formats, value mappings
  - Phase, power, frequency, polarization dimensions
  - Direct increment *vs*. “hopscotch” strides
- Explore alternate logics
  - Transformational (*vs*. gated) functions
  - Serial/temporal asynchronous functions
- Potential for multidimensional encoding
  - *vs.* multivalued 1D encodings
  - *e.g.*, concentric QAM *vs*. spiral QAM

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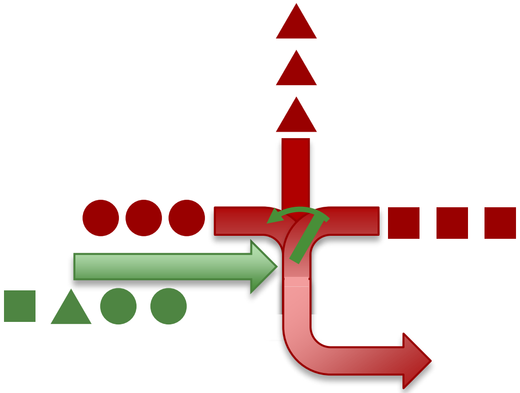
Functions

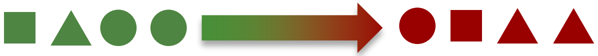
Gated functions

- Input selects other input(s) or constants (power rails)
- Requires constants, *i.e.*, symbol generation
- Requires clocking



Transformational functions

- Change input signal(s) into output signal(s)
- Self-synchronizing



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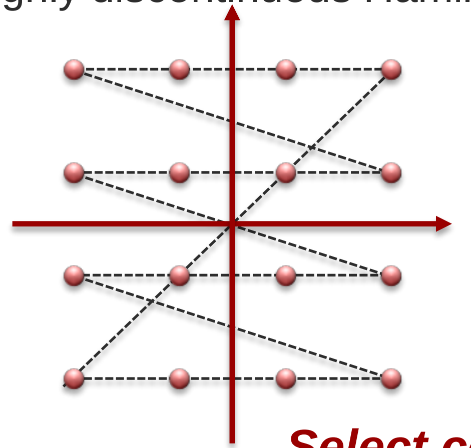
Coding

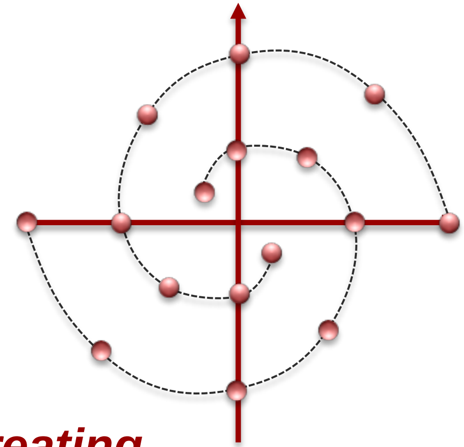
Current: Concentric QAM

- Uniform minimum distance between valid values
- Highly discontinuous Hamiltonian



OTM: Spiral QAM

- Value-independent transforms
- More continuous Hamiltonian



Select code and values creating a continuous Hamiltonian (path) via a constant transform

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New Models of Computation

- Extend logic for multibit optical symbols
  - What is required – a group?
    - As in Boolean NAND or NOR,
      but with more than just binary values
    - *E.g.*, modulus integers under add/multiply
  - Non-ring functions vs. full λ-calculus
- Explore opportunities for Turing Machine variant
  - Minimal functions for completeness
  - Is computation possible with ephemeral I/O?
    (maximum look-forward/back within fixed ΔT)
  - Is computation possible with ephemeral state?

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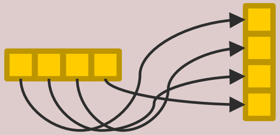
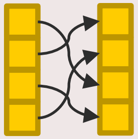
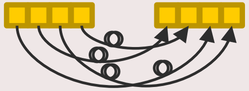
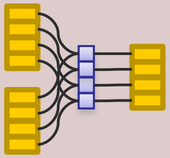
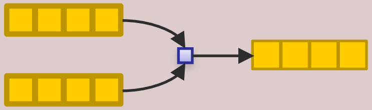
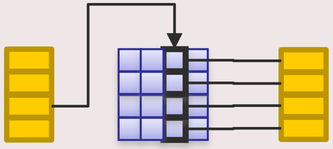
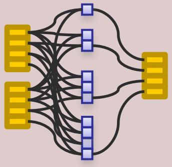
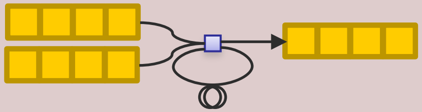
Exploring Functions:
Electronics vs. Optics

Input format	Convert to parallel 	✓ Serial data– native bit-stream
Permute	✓ Fixed permutations are wires. Variable permutations require switching 	Time-shift to permute. 1 nonlinear element, 1 delay per symbol Needs tuning, switching, timing 
XOR / Booleans	N 2-input gates in parallel 	✓ 1 function in series 
Table Lookup	✓Index into a table . Table data stored in memory or as fixed wires 	Tapped-line correlator to select from N pattern generators **Optical Tapped Delay Line**
Add	Full-lookahead devices. N lookahead functions, each of $O(N^2)$ elements 	✓ ✓ 1 function (6 elements), 1 delay 

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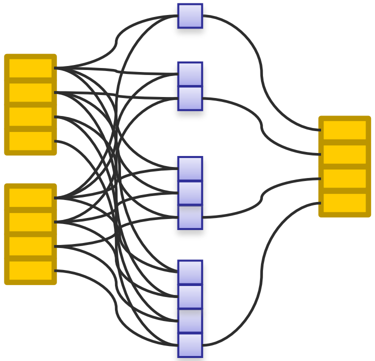
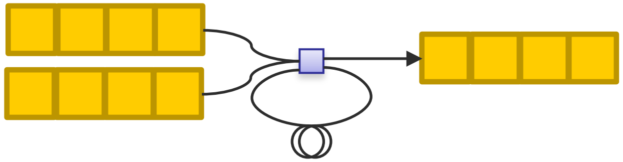
Adder Complexity

Electronics



Optics



- Parallel look-ahead (electronic) adder
  - Create, generate & propagate functions
    - $G_i = A_i B_i$
    - $P_i = A_i + B_i$
  - Compute carries
    - $C_{i+1} = G_i + P_i C_i$
    - $C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$
    - J^{th} element = OR of J groups of 1..J parts i.e., each element is $O(J^2)$
  - Total complexity is $O(N^3)$ for N-bit width
- Serial (optical) adder
  - Notation:
    - AND (adjacent), OR +, XOR ^
    - A, B = inputs; S = output
    - C = carry
  - Generate sum, carry (optical adder)
    - $S_i = A_i \wedge B_i \wedge C_{i-1}$
    - $C_i = A_i B_i + (C_{i-1}(A_i \wedge B_i))$
  - Total complexity is 6 (indep. of width)

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Core Areas of Investigation

- Multivalue symbol transformations
  - Multibit logic/math
    (rings/groups – poss. beyond boolean)
  - Symbol transforms – not gating
- Serialization
  - Serial logic/functions
  - Time-based (vs. space-based parallelism)
- Ephemeral state
  - Limited “lookback”
    (like USC/ISI Tetris router conveyor queues)

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Potential Impact

- On-line processing
  - Data too large/high-capacity (or both) for off-line proc.
- Low-power
  - Processing without OEO/SBS conversion
- Examples:
  - Checksums / error coding and correction
  - Encryption and authentication
  - Packet filtering / virus scans
  - Transcoding
  - Data fusion (merging stream info.)
  - Data reduction (map/reduce)

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Requirements

“Digital Transistor”, Miller, *Nature Photonics* 2010

1. Cascadable
   - Stage N output drives stage N+1 input
2. Fan-Out
   - Output can drive at least 2 inputs
3. Logic-level restoration
   - Re-digitization
4. Input/output isolation
   - Immune to reflection
5. Absence of critical biasing
   - Robust to configuration variation
6. Logic level indep. of loss
   - Robust to signal weakness

OTM

1. Digital (3) -> nonlinear
   - Requires re-digitization
2. **Persistent -> multibit & serial**
   - Space-P. = transmittable
   - Time-P. = storable
3. **Asynchronous -> transformational**
   - Functions transform inputs, not gate them
4. **Turing-equivalent**
   -> new math, alphabet, semantics
   - Recursive (operational induction) (1)
   - Time-Persistent
   - Group (two operations, *etc.*)
   - Conditionals
5. Robust? (4,5,6)
   - Stable under variation (*vs.* ECL?)

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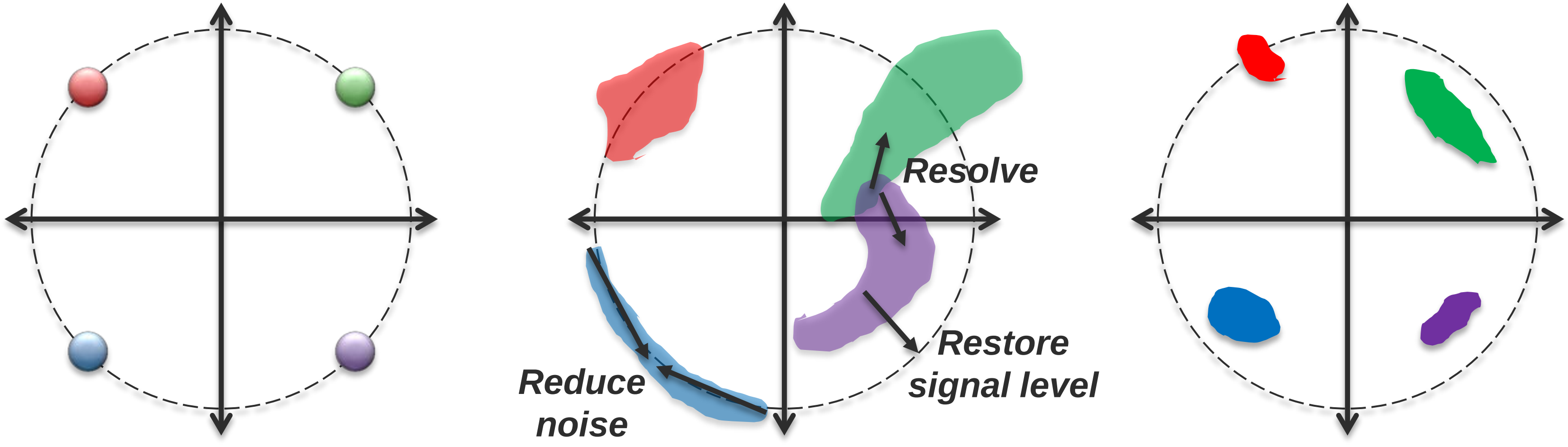
Re-digitization Challenge

- Reduce noise
  - Reduce variation in encoding domain - here phase, shown as angle
- Restore separation
  - Resolve overlap
- Restore signal level
  - Reamplify – here, power, shown as distance from origin



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Information Sciences Institute

Recent and Current Work

- Design of an all-optical IP packet router
  - Variable length messages (packets)
  - All-optical processing:
    1. ✓➔Decrement hopcount
    2. ✓ Match destination address to forwarding table
    3. ➔Recompute the IP checksum
    4. ✓ Merge packets sent to the same output port

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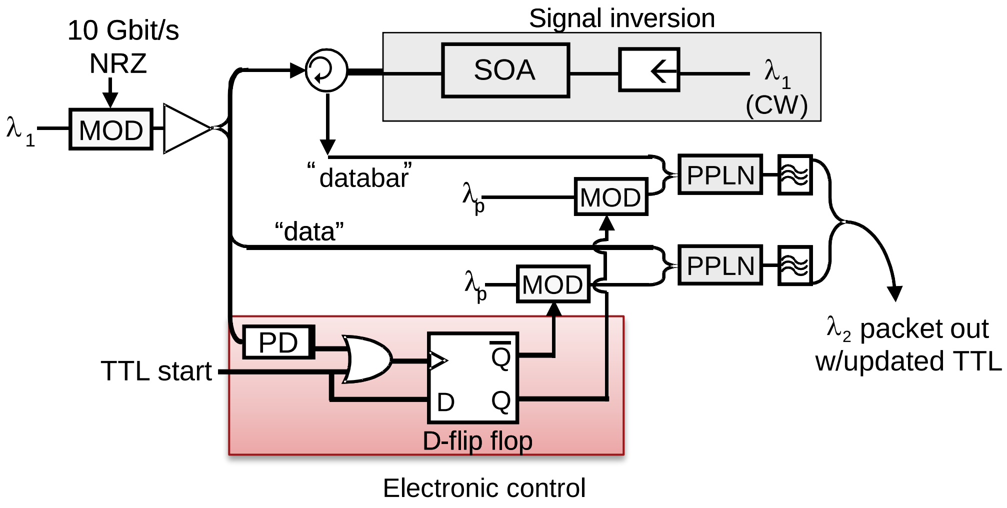
1. Hopcount Decrement

McGeehan et al., JLT 2003

- Serial unsigned decrement
  - Least-significant bit (LSB) first input
  - Invert (S=0 becomes 1) until S=1
  - Invert that bit (S=1 becomes 0)
  - Copy remaining bits
- Uses electronic control
  - Replace with laser, switch as RS flip-flop
- Multibit version:
  - LSS (symbol) input
  - S=0 becomes N-1 until S>0
  - S>0 becomes value-1
  - Copy remaining S



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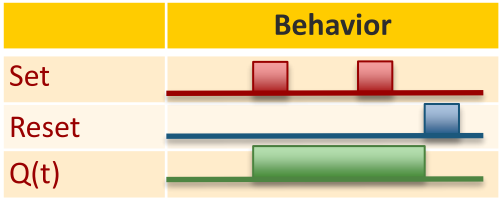
Hopcount Refinement

- Update to optical S/R FF
  - Previous design used electronic S/R FF
    - 2003 JLT paper
    - Set/reset:

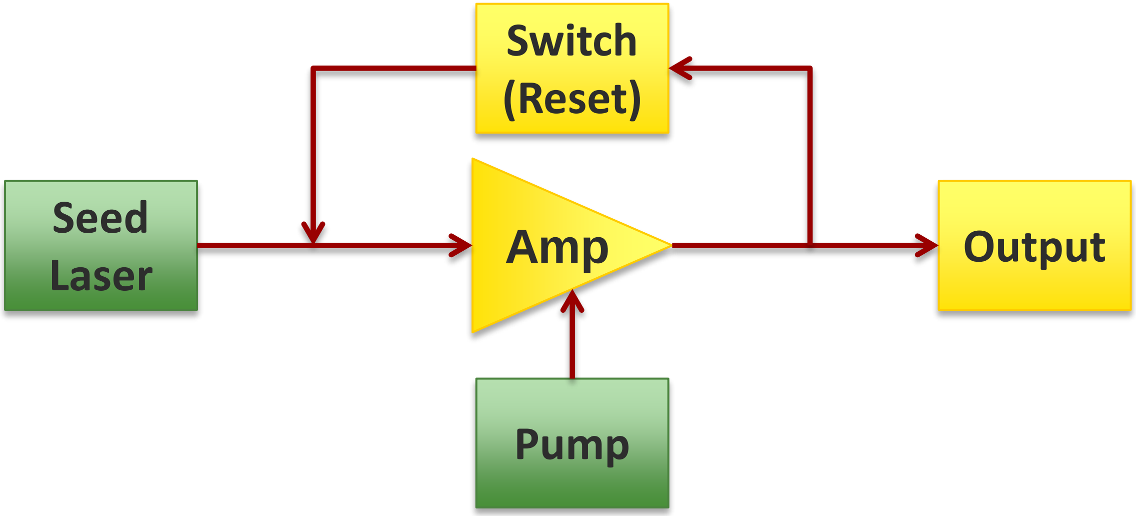


  - Optical FF design
    - Does not rely on phase interference
      - Extends beyond OOK/2PSK to symbol-encoding
- Extend to multibit encoding

Optical S/R FF

Current work

- Simulation (2010 REU students)
  - Compare variable seed *vs.* variable pump
- Implementation pending



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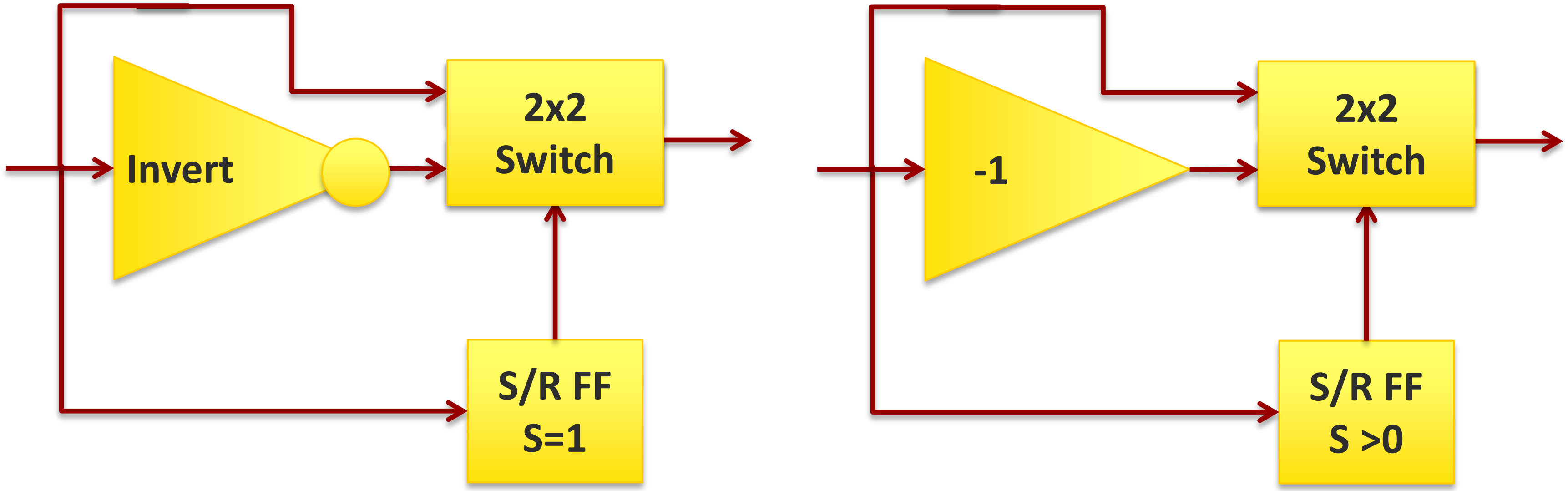
Decrement

Single-bit to multibit

- Invert becomes "-1" or "+(N-1)"
- S/R FF trigger becomes ">0"



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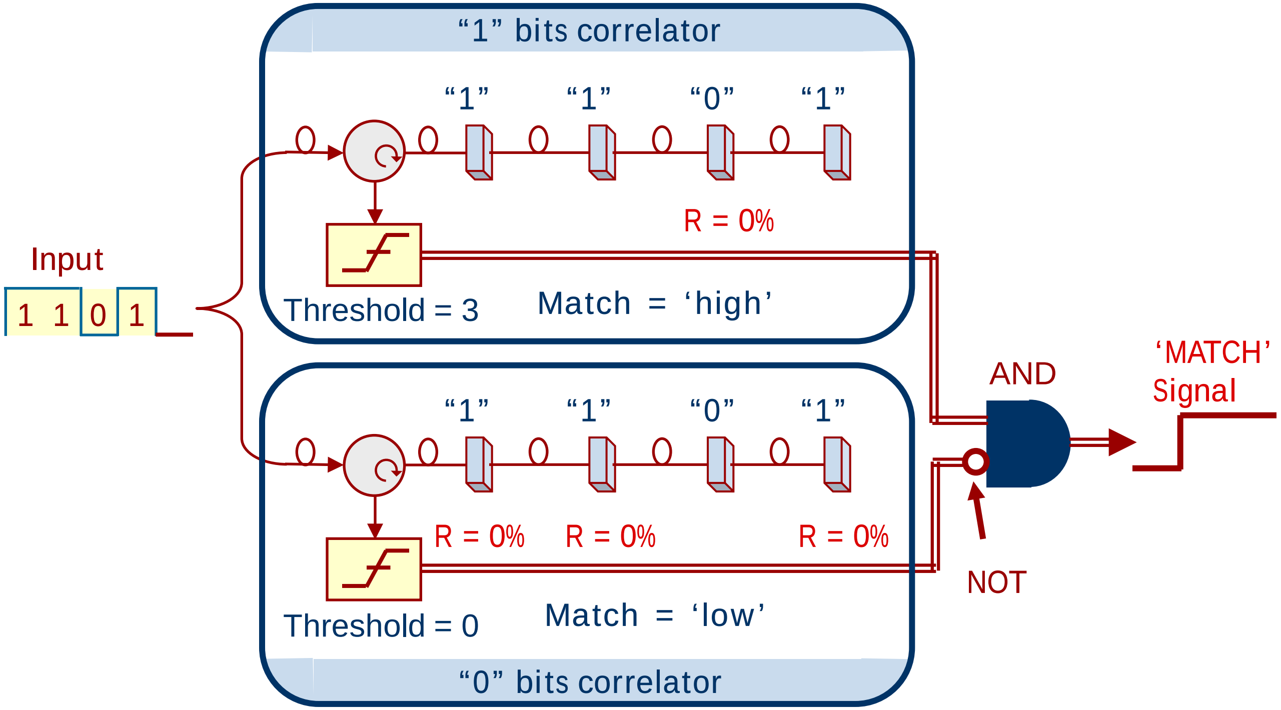
2. Match/Forward *via* Filters

Hauer et al., JLT 2003

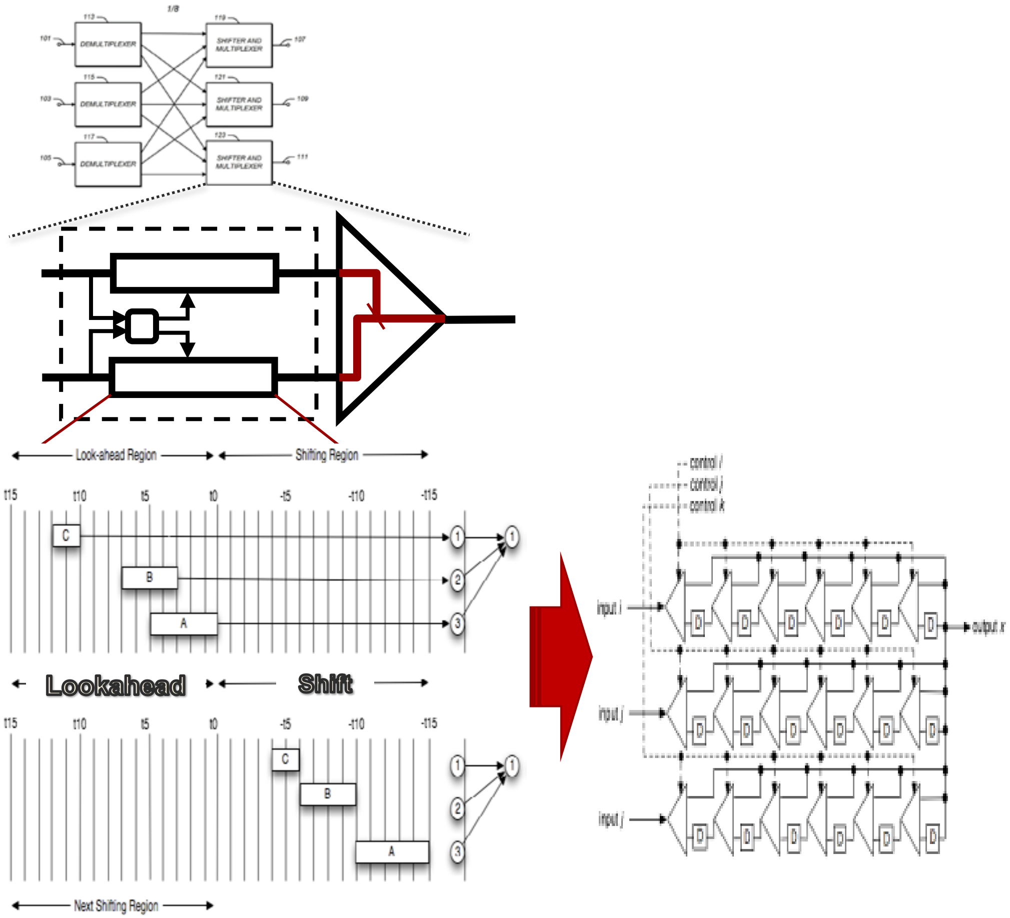
- **Bit-subset groups share next-hops**



4. Merging – Tetris

Touch et al., US Pat. 2012

- Conveyor queues
  - Variable speed
- Current results:
  - Better than backshift (Harai)
  - <4 packets delay
  - Batch scheduled



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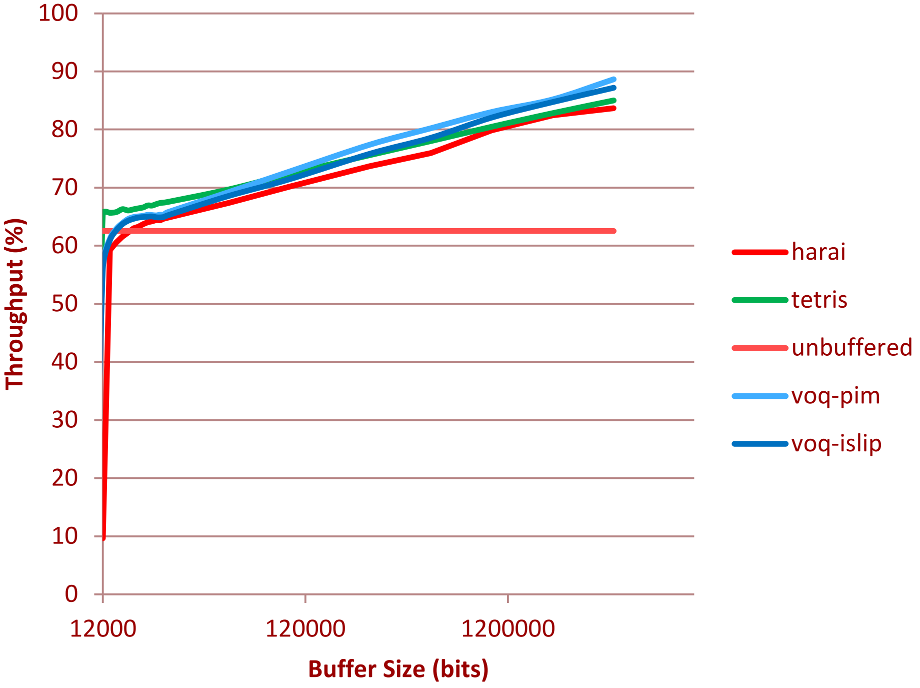
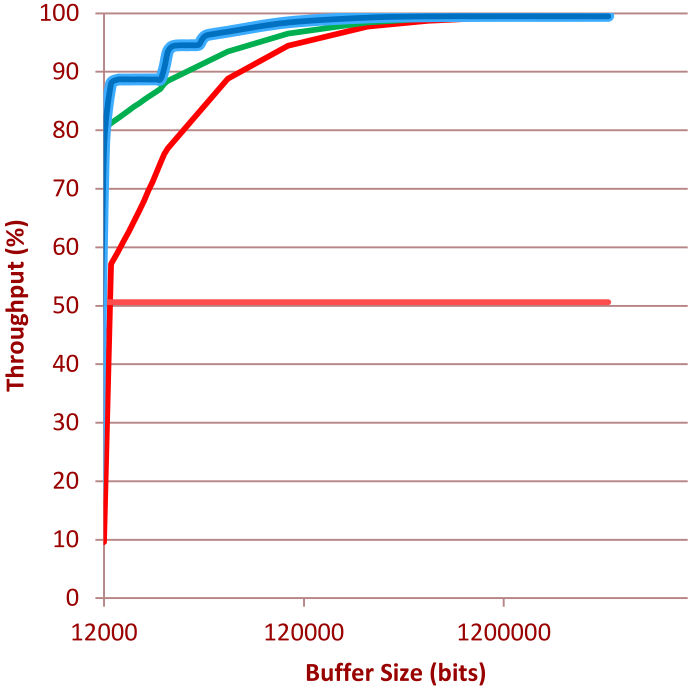
Tetris *vs.* NICT Comparison

- Simulation analysis – 32x32 switch @100% aggregate load
  - Tetris (shift-forward) *vs.* NICT (shift-backward) optical *vs.* VOQ-based electronic approaches

Pareto bimodal



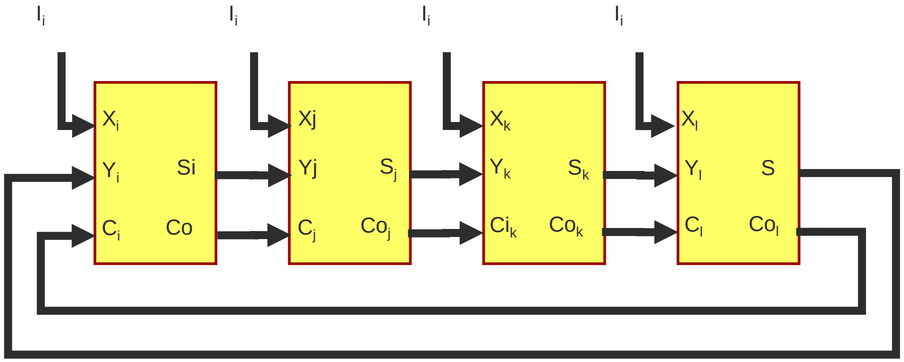
Poisson bimodal



3. Optical Checksum

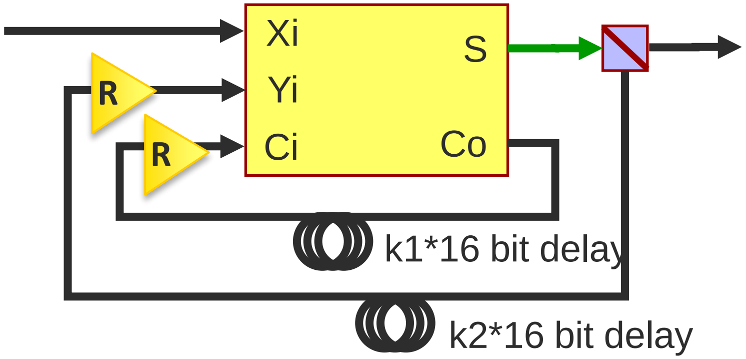
Current work

- Ones-complement sum
  - Symmetric – carry-out cascades to all other bits
  - Typically implemented using twos-complement
    - OSUM(***x***,***y***,***N***) = ***x*** + ***y*** + (carry(***x*** + ***y***) >> ***N***)
  - Same design for one-bit and multibit



Native Parallelized Checksum

Touch/Parham 1996



Serial Checksum

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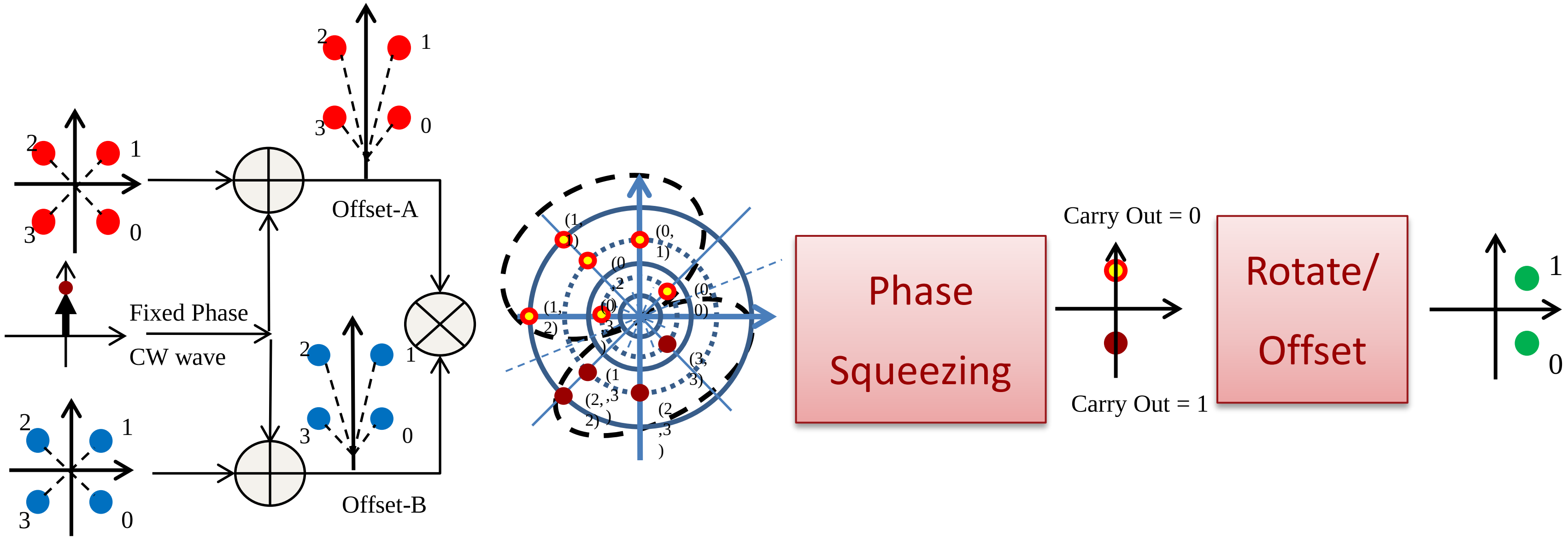
Multibit Half-Adder

- Extends modulus-adder(*Bogoni et al., 2009*)
  - Needs native carry-out that generates reusable values
  - Student poster award at OIDA Data Center Workshop



Phase Squeezing

Rotate/ Offset

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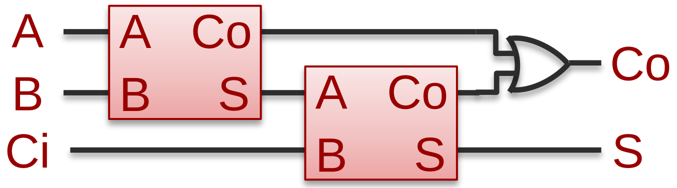
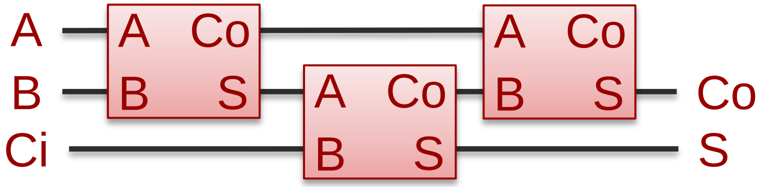
Half-Adder to Full-Adder

- Cascade adders – requires multibit design



Binary full-adder



Multi-bit full-adder

NB: final Co cannot occur

- Native design
  - Using PPLN/PPSI devices
  - No need for cascade of multiple devices

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Current Research Goals

- Implement/integrate
  - Hopcount decrement
  - IP checksum
  - Tetris aggregator (shift/merge)
- Design
  - Multibit symbol redigitizer
  - Multibit symbol functions

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OTM Summary

- New approach to computation
  - Designed to native constraints of transmission
  - First-principles revision to new domain
- Symbol-based
  - Concurrent coding, function, and physical realization
- Collaborators:
  - Prof. Alan Willner, USC EE/Systems
  - Ph.D. students: Mortezza Ziyadi,
Salman Khaleghi, Mohammed Reza Chitgarha

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